

Broad-Band Distributed Amplifier Impedance-Matching Techniques

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Abstract — A circuit concept is developed which allows impedance transformations to be performed over extremely broad bandwidths. The transformation is obtained by coupling one or more input or output lines of a distributed amplifier into several output or input lines respectively. The circuit technique is demonstrated for a 1:2 impedance transformation over a 2–20 GHz bandwidth by results presented for a fabricated amplifier. The amplifier yields a *VSWR* of better than 1.7:1 at the input into $25\ \Omega$ and better than 1.5:1 into $50\ \Omega$ at the output while maintaining a gain of $9 \pm 1\ \text{dB}$. An application of the technique to the important broad-band impedance-matching problem of a laser diode is discussed.

I. INTRODUCTION

IN ORDER TO prevent system degradation due to signal reflection, it is often necessary in microwave design to provide an impedance transformation having good return loss characteristics between a mismatched source and load. The transformation can be accomplished passively by several methods. One method consists of the use of a quarter-wavelength transformer of the appropriate length placed between the mismatched input and output. The performance of the transformer, however, is very dependent on the designed circuit wavelength; therefore only narrow-band impedance transformations are possible. An impedance-matching transformer having windings whose characteristic inductive impedance matches that of the respective input and output loads can also be used; however, transformers of this sort are limited to lower frequencies, have very limited bandwidth potential, and are very difficult to fabricate monolithically. Matching networks composed of passive elements can be used to achieve slightly wider bandwidths; however, the number of resonators becomes prohibitive as the bandwidth becomes wide and the transformation ratio becomes large. A method of providing this transition actively is to use reactively tuned amplifiers which are matched to different impedances at input and output. The bandwidth of these circuits is, however, limited by the potential of the reactive matching network, which is at most two octaves. Recently [1], interest has been renewed in distributed amplifiers due to their extreme bandwidth potential (as much as four to five octaves [2]) and easy producibility utilizing monolithic microwave circuit technology.

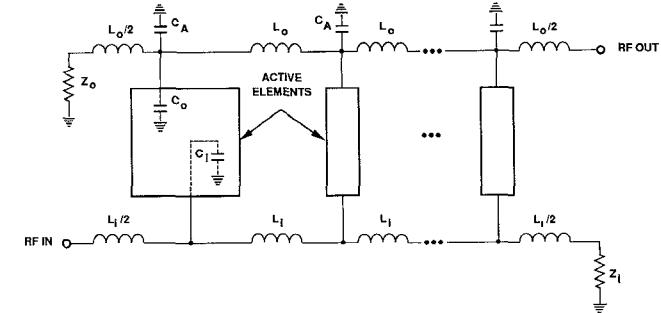


Fig. 1. General circuit used to realize a distributed amplifier.

Distributed techniques have been used to build broad-band mixers [3], frequency multipliers [4], and power splitters [5], as well as amplifiers [6]–[13]. Currently, the technology of distributed amplifiers has been focused on providing amplification between a source and a load with the same impedance. A technique is described here which exploits the bandwidth potential of distributed amplifiers in formulating a distributed impedance transformation amplifier. Variations of the technique are discussed for obtaining very large impedance ratios between input and output, including that necessary for driving a laser diode over more than four octaves of bandwidth.

II. GENERAL THEORY

The concept of distributed amplifiers revolves around the circuit shown in Fig. 1. The intent of this circuit is to combine active elements and passive components in such a manner as to form transmission line-like structures, thereby taking advantage of the properties of transmission lines, e.g., large bandwidth and gain flatness. As can be seen in Fig. 1, an input synthetic transmission line is formed by combining the shunt input capacitance of the active element with an appropriate amount of series inductance. The amount of added inductance is determined by the desired characteristic impedance at the input. Gain is realized by synthesizing a second transmission line containing the amplified signal at the output using the combined output capacitance of the active element, C_o , and an added capacitance, C_A , as the shunt element. The value C_A and the series inductance of the output line, L_o , are determined by stipulating that the phase velocities of the

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input and output synthetic transmission lines be equivalent, or [1]

$$v_{pi} = \left[1 - \left(\frac{f}{f_{ci}} \right)^2 \right]^{1/2} / [L_i C_i]^{1/2}$$

$$= v_{po} = \left[1 - \left(\frac{f}{f_{Co}} \right)^2 \right]^{1/2} / [L_o (C_o + C_a)]^{1/2} \quad (1)$$

where

$$f_{ci} = \frac{1}{\pi (L_i C_i)^{1/2}} \quad (2a)$$

$$f_{Co} = \frac{1}{\pi [L_o (C_o + C_a)]^{1/2}} \quad (2b)$$

and f is the frequency. This condition must be satisfied in order for the input wave to be coupled in phase to the output wave through the active elements along the length of the amplifier.

The characteristic impedances of the input and output synthetic transmission lines are also dependent on the values of the added inductance and capacitance and are given approximately by

$$Z_i = \left(\frac{L_i}{C_i} \right)^{1/2} \left[1 - \left(\frac{f}{f_{ci}} \right)^2 \right]^{1/2} \quad (3a)$$

and

$$Z_o = \left(\frac{L_o}{C_o + C_a} \right)^{1/2} \left[1 - \left(\frac{f}{f_{Co}} \right)^2 \right]^{1/2}. \quad (3b)$$

If the input and output impedances of the amplifier are chosen to be equivalent, then simultaneous solution of (1) and (3) results in $L_i = L_o$ and $C_i = C_o + C_a$. These equations form the basis of the determination of the necessary additive element values in a distributed amplifier.

III. IMPEDANCE TRANSFORMATION TECHNIQUES

A. Line Impedance Variation (LIV)

A simple method of obtaining a small impedance transformation from the input to the output is to adjust the elements along the input and output amplifier lines to reflect the desired impedances while adhering to the condition described by (1). Substituting the impedance transformation given by

$$Z_i = r Z_o \quad (4)$$

into (1) and (3) yields

$$C_a = r C_i - C_o \quad (5a)$$

and

$$L_o = L_i / r. \quad (5b)$$

Although adequate for small impedance transformations, the technique becomes inappropriate for larger

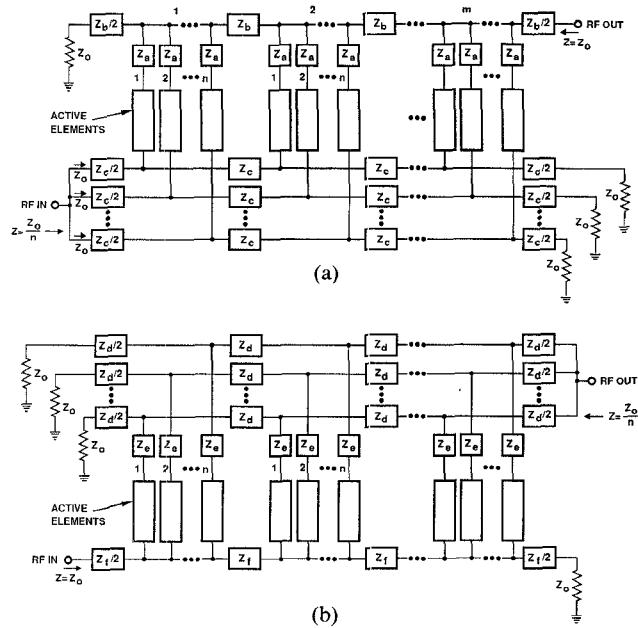


Fig. 2. Generalized circuit topology of the CLI distributed impedance transformation amplifier introduced in this paper. Amplifier configurations are shown for (a) an impedance multiplication and (b) an impedance division.

transformations for several reasons. For small values of r ($r < 0.33$ to 0.25), the value of the added capacitance C_a necessary for the transformation in (5) will become negative, precluding the possibility of transformations of magnitude greater than 1:3 to 1:4. Another problem with this technique is that the output or input transistor may be largely mismatched because of the impedance it must see in order to create a particular characteristic impedance along the output or input synthetic transmission line. The resulting circuit will have reduced circuit gain and increased noise figure and in many cases may even become unstable. Yet another problem will result for large transformations in that the large inductors and small capacitors (for large characteristic impedance) or small inductors and large capacitors (for small characteristic impedance) necessary to perform the required transition may become hard to realize physically. These extreme values of the circuit elements also cause the circuit to become more sensitive to process variations, as will be discussed in Section IV. These problems are eliminated by the use of the technique described below.

B. Constant Line Impedance

The generalized constant line impedance (CLI) circuit concept introduced here is described in Fig. 2. The two possible types of transformations (step up and step down) between the input and output are shown separately in the diagram. Fig. 2(a) describes the distributed CLI impedance transformation amplifier which is matched to a larger impedance at the output than at the input. In this structure, the input signal is split between n parallel distributed amplifiers, all having an input impedance of Z_o determined by the value of the series element Z_c and the shunt

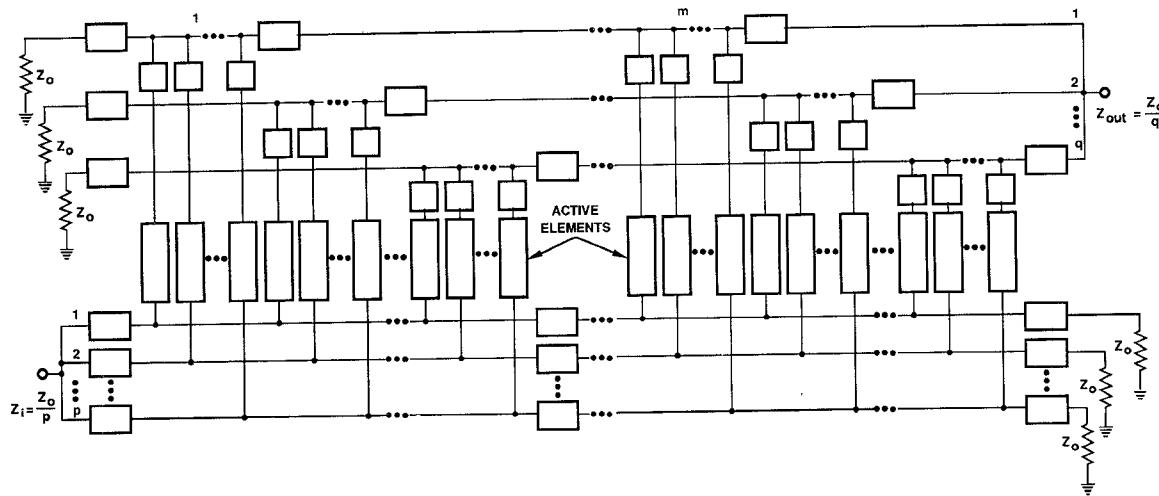


Fig. 3. Circuit topology for a CLI distributed impedance transformation amplifier which obtains an impedance transformation from input to output of $q:p$.

capacitance of a single active element. The resulting input impedance of the entire circuit is thus equal to Z_o/n . All of the parallel amplifiers have a common output line with the passive elements along this line, Z_a and Z_b , adjusted so that the impedance and phase velocity of the collective output line match those of each of the input lines. There are thus $n+1$ synthetic transmission lines, n input lines and 1 output line, all having identical properties. The impedance at the output is equal to the characteristic impedance of the single output line, Z_o .

The circuit of Fig. 2(b) achieves signal amplification between a source with a larger impedance than the load. All of the coupled distributed amplifiers have the same input line, whose characteristic impedance, Z_o , is set by the value of Z_f and the parallel combination of the n shunt active elements. The values of Z_d and Z_e are adjusted so that the phase velocity and characteristic impedance of the output lines match those of the common input line. The output lines of the amplifiers are attached in parallel at the output, resulting in an output impedance of Z_o/n . Thus, as in the previous circuit, there are $n+1$ synthetic transmission lines, all having the same properties; in contrast, however, there are n output lines and 1 input line, resulting in impedance reduction at the output.

Impedance transformations of other than integral multiples can be obtained in either of two ways. The CLI technique can be used by incorporating both the step-up transformation and the step-down in the same circuit, as described by Fig. 3. In this circuit p input arms are coupled to q output arms to obtain an impedance transformation of q/p . This technique for noninteger ratios is somewhat limited, however, as the number of active elements and corresponding synthetic transmission lines may become prohibitively large. A simpler method would involve combining both the LIV and CLI techniques simultaneously; e.g., a 2.5:1 transformation can be obtained by performing a 5:4 transformation using the LIV method on each of the arms of a 2:1 CLI impedance divider. The

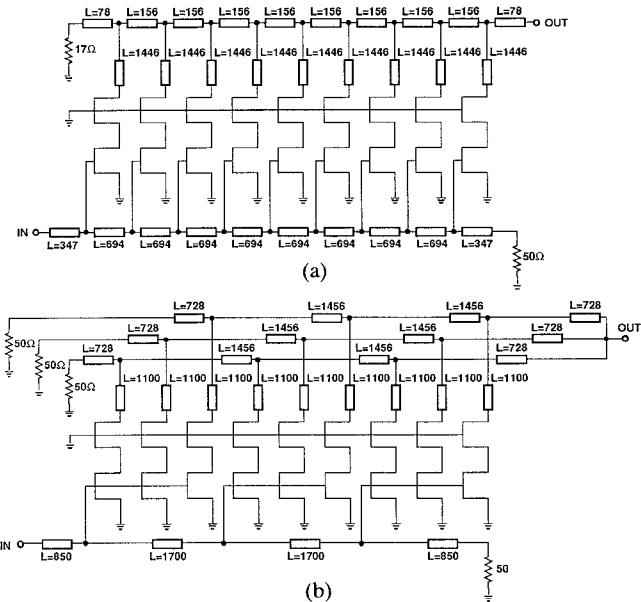


Fig. 4. Circuit topologies and element values for a 3:1 wide-band distributed impedance division using (a) the LIV method and (b) the CLI method.

combination of techniques can also be used to obtain large impedance transformations, as will be discussed in Section VII.

IV. SIMULATED COMPARISONS OF THE LIV AND CLI TECHNIQUES

A comparison of the LIV method and the CLI method was performed through simulation for a 3:1 impedance transformation. The simulated LIV circuit, illustrated in Fig. 4(a), consisted of nine cascode pairs. The output drain line of the LIV circuit was terminated in a $17\ \Omega$ load resistance and the input line was terminated in a $50\ \Omega$ resistance, reflecting the characteristic impedances of each of the synthesized transmission lines necessary to yield the desired 3:1 transformation. The comparable CLI circuit is illustrated in Fig. 4(b). In this case, all of the synthesized

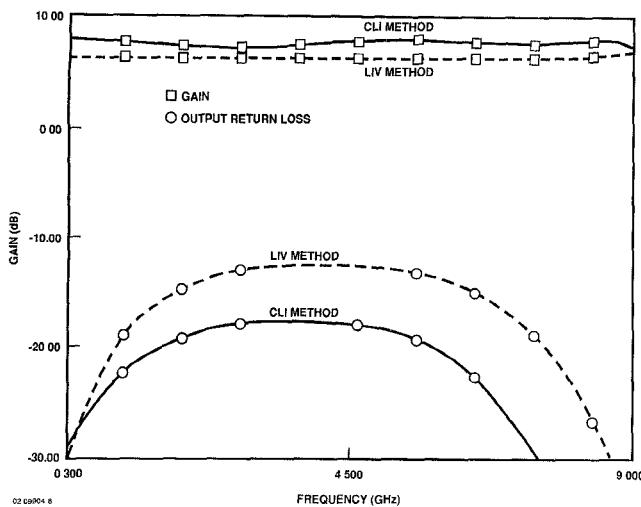
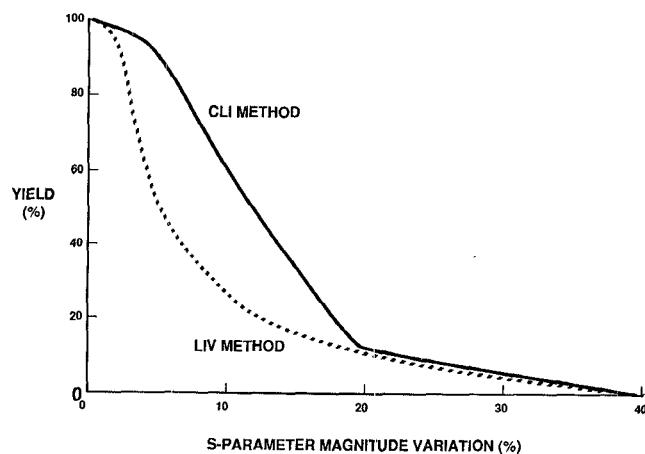


Fig. 5. Simulated responses for the circuits shown in Fig. 4. The LIV circuit response is shown as the dashed line.

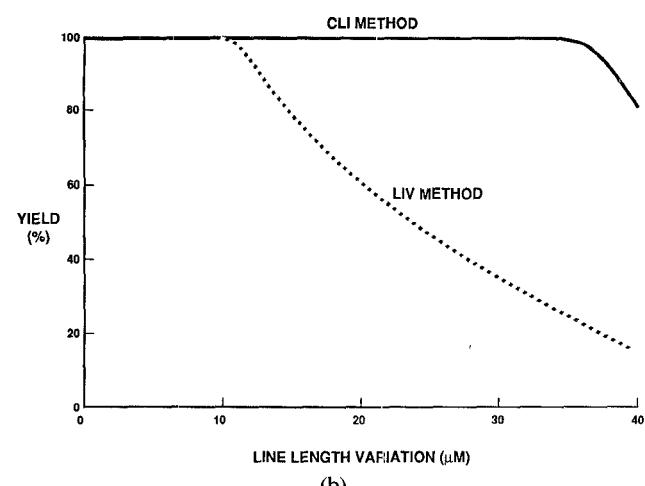
transmission lines are terminated in identical load resistances of 50Ω . For each simulation the transistor S parameters used were measured from Rockwell foundry $0.5\text{-}\mu\text{m}$ -gate-length and $180\text{-}\mu\text{m}$ -gate-width FET's. Both circuits utilize the same number of devices and thus the same total device area. The lengths of the microstrip transmission line elements were calculated in each case according to (1) to (5) and then optimized for highest gain and best output match.

Fig. 5 presents the simulated results of the circuits shown in Fig. 4. The CLI technique yields an approximate improvement in gain of about 2 dB and a return loss improvement of between 5 and 15 dB over the LIV technique across the circuit bandwidth. Additionally, the asymmetries of the LIV circuit shown in Fig. 4(a) make it more difficult to realize physically than the CLI circuit shown in Fig. 4(b). For this reason impedance transformations larger than 3:1 must be performed using the CLI technique. Stability is also improved using the CLI technique. The LIV circuit becomes conditionally stable at around 12.5 GHz whereas the CLI circuit remains unconditionally stable with a stability factor greater than 3 for all frequencies. It should be mentioned that the bandwidth of the circuit of Fig. 5(b) is slightly reduced due to the additional shunt capacitance introduced by the CLI method on the input synthetic transmission line for step-down transformations. This capacitance can be reduced and the bandwidth correspondingly increased by using a capacitor placed in series with the shunt transistors, as demonstrated by Chase and Kennan [9] for high gate periphery power distributed amps or by the technique described in Section IV. For step-up impedance transformations, the CLI technique results in increased bandwidth because of the reduced series inductance on the input line.

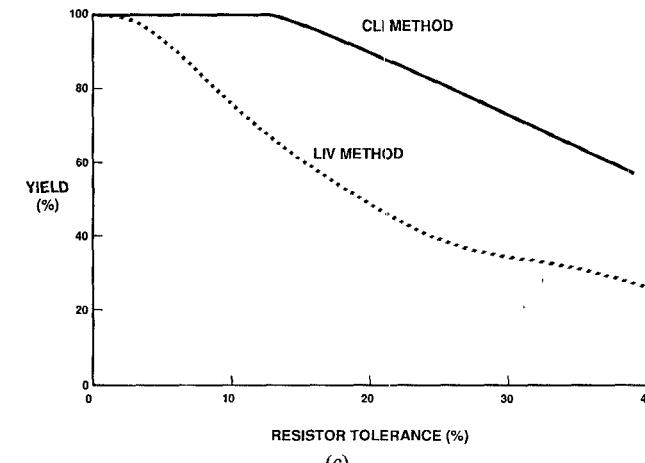
Monte Carlo yield simulations were also performed on the circuits described by Fig. 4. In both cases, a circuit was considered a failure if its gain dropped by more than 10 percent of the predicted value or if the magnitude of the input or output return loss degraded by more than 20



(a)



(b)



(c)

Fig. 6. Circuit yield is simulated for statistical variation of (a) transistor S parameters, (b) microstrip line length, and (c) sheet resistance for both the LIV and CLI impedance transformation methods.

percent. Fig. 6 describes the results of statistically varying each of the important process parameters involved. In each case, all other process parameters were kept constant. The graphs clearly demonstrate the vast superiority of the CLI method for overall circuit yield. The reduced yield of the LIV circuit is due to the extremely small inductance values necessary to create the output transmission line imped-

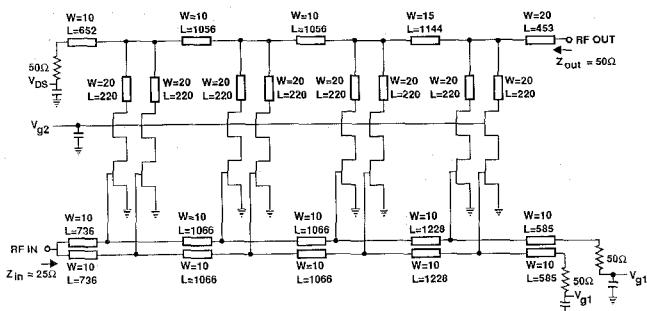


Fig. 7. Circuit diagram and element values for a circuit designed and fabricated using the CLI technique.

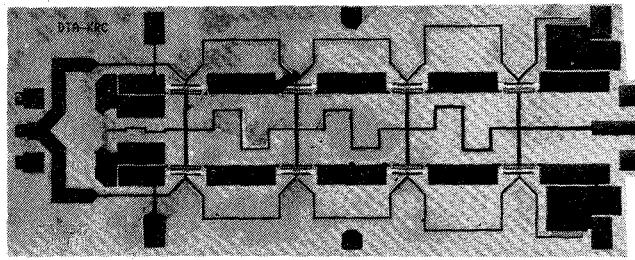


Fig. 8. Photograph of the fabricated wide-band CLI distributed impedance transformation amplifier.

ance, and the more severe mismatching of the output transistor over the CLI technique.

A limitation of both the LIV and the CLI technique is that impedance transformations can be obtained only between input and output impedances which are smaller than the impedances of any of the amplifier synthetic transmission lines. Thus, impedance transformations between large impedances would be limited by the ability to design the amplifier to have large characteristic impedances along the synthetic transmission lines.

V. RESULTS

A circuit which demonstrates the transformation described by Fig. 2(a) was designed, simulated, and fabricated. The impedance transformation occurs between an input impedance of $25\ \Omega$ and an output impedance of $50\ \Omega$. Optimized circuit element values are shown in Fig. 7. The active element is a cascode connected pair of $0.5\text{-}\mu\text{m}$ -gate-length GaAs FET's. The passive elements are transmission lines whose lengths are adjusted to yield maximum gain and minimum return loss. The transistor widths for the devices used in the simulations are $180\ \mu\text{m}$, which was determined to be the optimum width for the desired $2\text{--}20\ \text{GHz}$ bandwidth. The common-source FET was designed using a split source to bring out the gate connection (as in the pi fed structure) whereas the common-gate device has gate connections on both sides to bypass capacitors. The novel dual FET structure results in minimized parasitic capacitances and allows easy incorporation into the circuit layout.

A photograph of the completed circuit is shown in Fig. 8. The circuit was probed on wafer with a Cascade probe, and circuit S parameters were measured with an HP8510 network analyzer. The measured input and output impe-

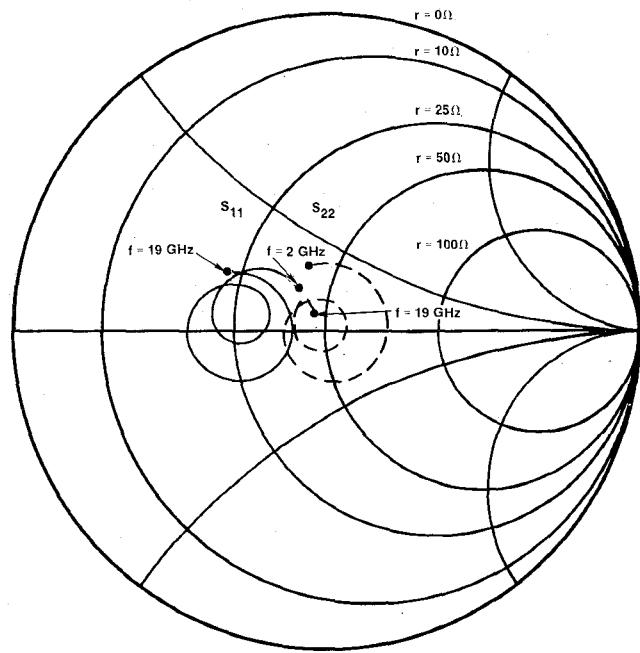


Fig. 9. Measured input and output impedances of the impedance transformation amplifier plotted on a $50\ \Omega$ Smith chart from 2 to $19\ \text{GHz}$.

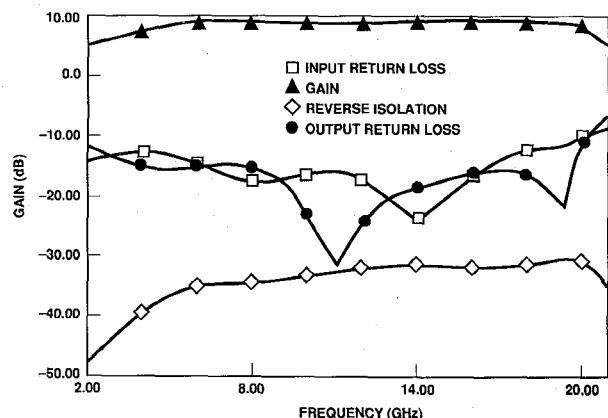


Fig. 10. Measured S parameters of the distributed impedance transformation amplifier terminated in a $25\ \Omega$ input impedance and a $50\ \Omega$ output impedance.

dances of the amplifier are shown on the normalized $50\ \Omega$ Smith chart shown in Fig. 9. The chart clearly illustrates that the amplifier input impedance remains close to the value of $25\ \Omega$ whereas the output impedance is approximately $50\ \Omega$ over the frequency range from 2 to $19\ \text{GHz}$. In order to obtain a true plot of gain and return loss, the S parameters measured in a $50\ \Omega$ environment must be translated via circuit simulation to reflect a $25\ \Omega$ input termination. The measured and translated parameters were very similar except for the value of the input return loss, which is significantly less for a $25\ \Omega$ input termination than for the $50\ \Omega$ termination of the measuring system, as expected. The resulting translated parameters are shown in Fig. 10. The circuit obtains a gain of $9 \pm 1\ \text{dB}$ from 4 to $20\ \text{GHz}$ and a return loss at the input and output of more than $12\ \text{dB}$ from 2 to $19\ \text{GHz}$. The dc drain bias was $150\ \text{mA}$ at $4\ \text{V}$ for a total dc power consumption of $600\ \text{mW}$. The 1 dB compression point was measured to be greater than $20\ \text{dBm}$ at $9\ \text{GHz}$.

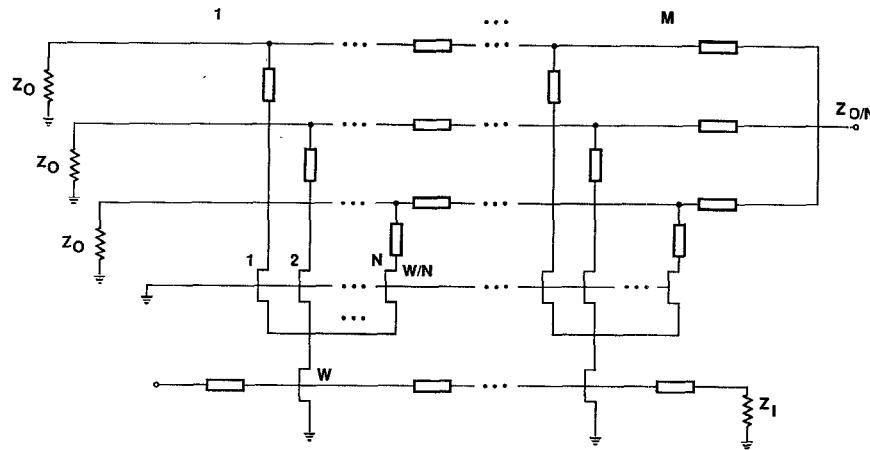


Fig. 11. Extension of the CLI technique for step-down impedance transformations. The modification improves the bandwidth and total dc power consumption of the circuit.

VI. CIRCUIT TOPOLOGY VARIATIONS FOR LARGE IMPEDANCE TRANSFORMATION

For very large high-to-low impedance transformations, application of strictly the CLI method becomes impractical because of the large capacitance attained on the input transmission line. This large capacitance ultimately limits the bandwidth and can reduce circuit yield dramatically. In addition, a large dc current is required to power the large number of parallel transistors in the circuit. A circuit topology which eliminates these problems is illustrated by Fig. 11. In this circuit, the common-gate FET of the cascode pair in the step-down CLI circuit is replaced by n source coupled common-gate FET's, each with a gate width that is $1/n$ times the gate width of the common-source FET. The smaller gate widths of the common-gate FET's are required in order to match the dc current of the common-source FET to that of the aggregate common-gate FET's. The high output impedance of the common-gate FET is sufficient to isolate each of the output drain lines from one another, resulting in a total output return loss approaching that of the strict CLI technique. The dc power required to operate the circuit is, however, reduced by a factor of n . Additionally the bandwidth is theoretically increased by a factor of n . There are limits, however, on the number of common-gate FET's that can be placed in series with the common-source FET. The necessary decrease in size of each common-gate transistor with each additional FET placed in parallel with it results in a higher output impedance of each FET and a correspondingly degraded output gain match with the output line. This factor must be taken into account in the design of large impedance transformations such as that discussed in the following section.

VII. SIMULATION EXAMPLE—THE BROAD-BAND LASER DIODE DRIVER

The technique described in the previous section can be aptly demonstrated by considering a situation for which there is currently no solution—that of a broad-band matching circuit for a semiconductor laser diode. A circuit accomplishing the necessary 8:1 impedance transforma-

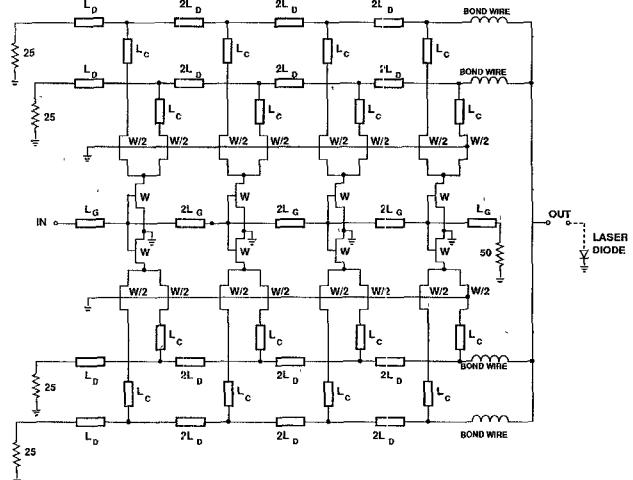


Fig. 12. Circuit diagram of the wide-band laser diode matching circuit example. The gate width W equals $200 \mu\text{m}$ and the optimized line lengths are $L_D = 150 \mu\text{m}$, $L_C = 1365 \mu\text{m}$, and $L_G = 400 \mu\text{m}$.

tion from an input of 50Ω to a typical laser diode impedance of 6.25Ω is described by Fig. 12. The 8:1 transformation is obtained by applying the extended CLI technique to obtain a 4:1 transformation, with the LIV technique providing the additional 2:1 transformation on each of the arms. Although the input impedance of a laser diode is not purely real, it can be accurately represented by a series RL circuit at high frequency because the internal and parasitic capacitances of the diode are swamped out by the bond wire inductance. In order to account for the bond wire, the final inductance of each of the arms of the distributed impedance transformation amplifier becomes the bond wire inductance.

Simulated results of the broad-band laser driving circuit are shown in Figs. 13 and 14. The circuit obtains a gain of $8.5 \pm 1 \text{ dB}$ from 0.5 to 12.5 GHz and better than 10 dB return loss at both the input and the output. The transistor S parameters used in the simulation were measured from $200\text{-}\mu\text{m-gate-width}$ and $0.25\text{-}\mu\text{m-gate-length}$ AlGaAs HEMT's. Variation of the bond wires lengths from 1 to 1000 μm resulted in less than 1 dB degradation in gain and less than 4 dB degradation in output return loss. Input

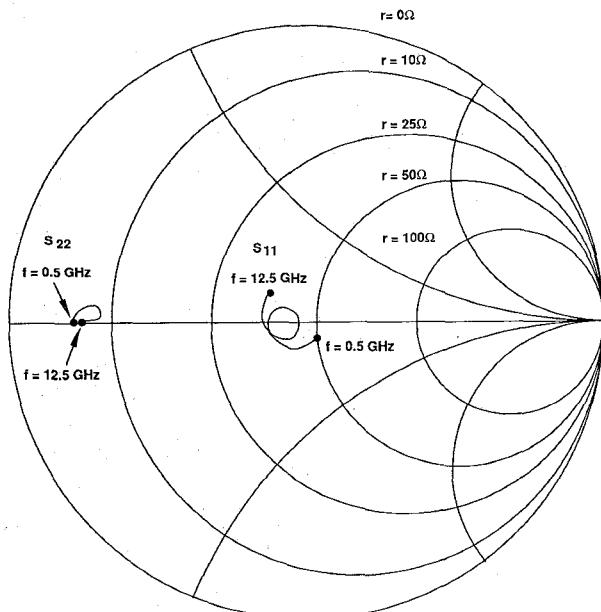


Fig. 13. Simulated input and output impedance of the wide-band laser diode matching circuit example plotted on a $50\ \Omega$ Smith chart.

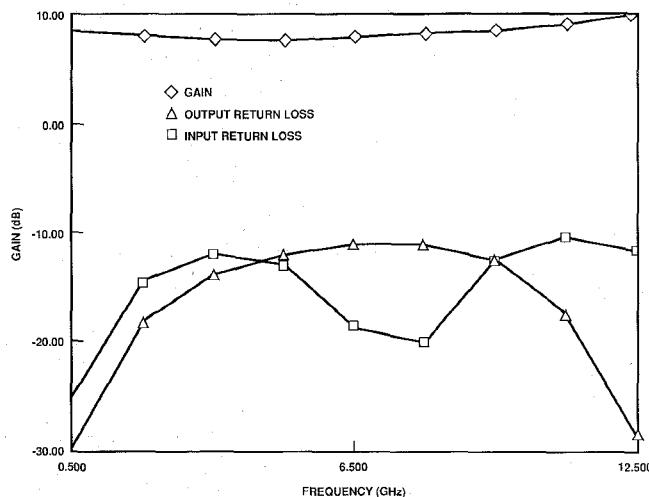


Fig. 14. Simulated gain and return loss of the wide-band laser diode matching circuit example.

return loss was unchanged. Gain for the circuit remained flat independent of the bond wire length. The simulation example clearly illustrates the potential of the technique in matching extreme impedance variations over large bandwidths.

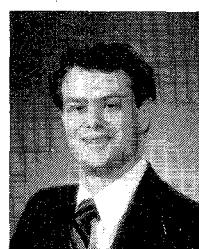
VIII. CONCLUSIONS

An active circuit design technique which allows impedance transformations over extremely broad bandwidths has been described and demonstrated. Potential uses for the distributed impedance transformation amplifier include wide-band RF semiconductor laser and optical modulator driver circuits (impedance division), broad-band front-end receiver circuits which match antennas with characteristic impedances greater than $50\ \Omega$ to $50\ \Omega$ circuits (impedance division), and wide-band transmitters

where the transmitting antenna impedance does not match the circuit impedance (impedance multiplication). An example of an 8:1 impedance divider suitable for driving a laser diode was discussed. In general the idea can be applied to almost any matching application where wide bandwidths are required.

REFERENCES

- [1] W. Keenan and N. K. Osbrink, "Distributed amplifiers: Their time comes again," *Microwaves and RF*, pp. 119-126, Nov. 1984.
- [2] R. Pauley, P. G. Asher, J. M. Schallenberg, and H. Yamasaki, "A 2-40 GHz, monolithic distributed amplifier using dual-gate GaAs FETs," in *GaAs IC Symp. Dig.*, Nov. 1985, pp. 15-17.
- [3] T. S. Howard and A. M. Pavio, "A distributed monolithic 2-18 GHz dual-gate FET mixer," in *IEEE Microwave and Millimeter-Wave Monolithic Circuits Symp. Dig.*, 1987, pp. 27-30.
- [4] A. M. Pavio, S. D. Bingham, R. H. Halladay, and C. A. Saphe, "A distributed broadband monolithic frequency multiplier," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 1988, pp. 503-504.
- [5] G. S. Barta, K. E. Jones, G. C. Herrick, E. W. Strid, "A 2 to 8 GHz leveling loop using a GaAs MMIC active splitter and attenuator," in *IEEE Microwave and Millimeter-Wave Monolithic Circuits Symp. Dig.*, 1986, pp. 75-79.
- [6] R. Larue, S. Bandy, and G. Zdziarski, "A high gain, monolithic distributed amplifier using cascode active elements," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 1986, pp. 23-26.
- [7] R. McKay and R. Williams, "A high performance 2-18.5 GHz distributed amplifier, Theory and Experiment," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 1986, pp. 27-31.
- [8] A. Cappello *et al.*, "A high performance, quasi-monolithic 2 to 18 GHz distributed GaAs FET amplifier," in *IEEE MTT-S Int. Microwave Symp. Dig.*, June 1987, pp. 833-836.
- [9] E. Chase and W. Kennan, "A power distributed amplifier using constant- R networks" in *IEEE MTT-S Int. Microwave Symp. Dig.*, June 1986, pp. 13-17.
- [10] R. Halladay, M. Jones, and S. Nelson, "A producible 2 to 20 GHz monolithic power amplifier," in *IEEE Microwave and Millimeter-Wave Monolithic Circuit Symp. Dig.*, 1987, pp. 19-21.
- [11] J. Orr, "A stable 2-26.5 GHz two-stage dual-gate distributed MMIC amplifier," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 1986, pp. 19-22.
- [12] C. Hutchinson and W. Keenan, "A low noise distributed amplifier with gain control," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 1987, pp. 165-168.
- [13] Y. Ayasli, L. D. Reynolds, R. L. Mozzi, and L. K. Hanes, "2-20 GHz traveling-wave power amplifier," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-32, pp. 290-295, Mar. 1984.



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Since joining Rockwell in 1987, he has been responsible for low-temperature HEMT characterization, MMIC design, active device and passive component modeling, and the application of optical devices to microwave systems.